DELAY CIRCUIT AND METHOD

CROSS REFERENCE TO A RELATED APPLICATION

This is a Continuation of application Ser. No. 08/595,512, filed on Feb. 1, 1996, which has been abandoned, which is a continuation of Ser. No. 08/411,556, filed on Mar. 28, 1995, which has been abandoned, which is a Continuation In Part of Ser. No. 08/365,685, filed Dec. 29, 1994, and entitled A DELAY CIRCUIT AND METHOD, which is a pending application.

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates to electronic circuits used to delay signals and more specifically to circuits used to delay the turn-on of a power transistor in a bridge configuration.

2. Description of the Relevant Art

The problem addressed by this invention is encountered when power transistors are used to drive a prior art bridge configuration such as in FIG. 1. The bridge configuration 2 can be used to power motors, drive solenoids, and the like. The bridge configuration 2 is characterized by the high side driver transistor 4 being connected in series to a low side driver transistor 6 across the voltage of a power supply. In this configuration, node 12 is driven to the power supply voltage when the high side transistor 4 is on and transistor 6 is off. Conversely, node 12 is sunk to ground when high side transistor 4 is off and lowside transistor 6 is on. If the high side and low side transistors are both turned off, then node 12 is at a high impedance state. However, if both high side 4 and low side 6 transistors are turned on, then the transistors are shorting the power supply voltage to ground which would draw an excessive amount of current and would damage one or both of the transistors. The bridge configuration is never used with both high side and low side drivers on at the same time because of the potentially disastrous results. Consequently, it is common to use a delay circuit as part of the control logic in the control block 9 to prevent the turn-on of one driver transistor until the other driver is turned off. In principle, one of the drivers is turned off while the other driver is turned on, but only after the delay circuit has delayed the turn-on by an amount of time which will guarantee that the other driver is in fact turned off.

FIG. 2 illustrates a prior art delay circuit 20 used in the control block 9 of FIG. 1 for delaying the turn-on of the driver transistors 4 or 6. In delay circuit 20, p-channel transistor 22 and n-channel transistor 24 form a first inverter. Similarly, p-channel transistor 30 and n-channel transistor 32 form a second inverter. The gates of transistors 22 and 24 form the inputs of the first inverter and the drain of transistor 30 and the drain of transistor 32 form the output of the second inverter. In operation, as the input signal goes from a low voltage to a high voltage, transistor 22 turns off and transistor 24 turns on. As a result, the voltage at node 23 drops from near Vdd to near ground. Consequently, the charge on capacitor 28 is drained through resistor 26 and transistor 24. The rate of discharge is determined by the size of resistor 26 and capacitor 28 as is known in the art. When the voltage on node 31 reaches approximately 2.5 volts, transistor 32 turns off and transistor 30 turns on which raises the voltage at node 33. The time delay can be approximated by the equation:

$$T_{delay}=(R26)(C28)1n(1-Vdd/V_{threshold})$$

Therefore, the rising signal on the input of the delay circuit **20** is passed on to the output of the delay signal **33**, but only after the delay created by the time constant of resistor **26** and capacitor **28**. However, prior art delay circuit **20** is limited since it often requires relatively large capacitors and/or resistors to obtain long delays. The requirement of a large capacitor or resistor is undesirable since a large capacitor or resistor typically requires large amounts of silicon on an integrated circuit or requires an external connection for an external capacitor. Since the cost of a integrated circuit is directly proportional to the die size, it is desirable to reduce the size of a circuit whenever possible.

SUMMARY OF THE INVENTION

Therefore, it is an object of the invention to provide relatively long delays without requiring a large capacitor or a large resistor.

It is further an object of this invention to provide a delay circuit which provides relatively long delays and without requiring large area on an integrated circuit.

It is further an object of this invention to provide a delay circuit which reduces the cost of a delay circuit by reducing the die area necessary to implement the circuit.

These and other objects, features, and advantages of the invention will be apparent to those skilled in the art from the following detailed description of the invention, when read with the drawings and appended claims.

BRIEF DESCRIPTION OF THE DRAWING

FIG. **1** is a schematic drawing of a prior art bridge configuration.

FIG. **2** is a schematic drawing of a prior art delay circuit.

FIG. **3** is a schematic drawing of an embodiment of a delay circuit.

FIG. **4** is a plan view of a layout of an embodiment of the delay circuit on an integrated circuit.

FIG. **5** is a schematic drawing of the delay circuit with a programmable delay control.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Referring now to FIG. **3**, a delay circuit **40** constructed according to an embodiment of the invention will be described. The input of the delay circuit **40** is connected to the gate of P-channel transistor **48** and to the gate of a n-channel transistor **50**. The source of transistor **48** is connected to a voltage source Vdd and the drain of transistor **48** is connected to the gate of p-channel transistor **52**, to the gate and drain of p-channel transistor **42**, and to the first end of resistor **44**. The second end of resistor **44** is connected to the drain and gate of n-channel transistor **46**, to the gate of n-channel transistor **54**, and to the drain of n-channel transistor **50**. The sources of transistors **46**, **50**, and **54** are connected to a voltage reference, ground. The source of transistor **52** is connected to Vdd. The drain of transistor **52** is connected to the drain of transistor **54**, to the first plate of capacitor **56**, to the gate of p-channel transistor **58**, and to the gate of n-channel transistor **60**. The second plate of capacitor **56** is connected to ground. The source of transistor **58** is connected to Vdd. The source of transistor **60** is connected to ground. The drain of transistor **58** and the drain of transistor **60** are connected to the gate of p-channel transistor **62** and to the gate of n-channel transistor **64**. The source of transistor **62** is connected to Vdd. The source of transistor **64** is connected to ground. The drain of transistor **62** is con-

nected to the drain of transistor **64**, the connection thereof forms the output of the delay circuit **40**. Although the construction of this circuit is described using MOSFET transistors, it is understood in the art that a similar circuit can be constructed using bipolar transistors, and the like.

In operation, an input signal is received at the gates of transistors **48** and **50**. If the input signal is at a low voltage, transistor **48** turns on which allows for transistors **46** and **54** to conduct a constant current through transistor **54**. The constant current through transistor **54** discharges capacitor **56**. Conversely, capacitor **56** is charged when the input signal is at a high voltage since this high input voltage turns transistor **48** off and turns transistor **50** on. Therefore, transistors **46** and **54** are held off while transistors **42** and **52** are turned on. Thus, transistor **52** charges capacitor **56** with the constant current source formed by transistor **42**, resistor **44**, and transistor **52**. The voltage on capacitor **56** buffered to the output by two inverters formed with transistors **58**, **60**, **62**, and **64**. In short, an input signal is received by transistors **48** and **50**, delayed by the constant current sources or drains in combination with the capacitor, and then buffered by two inverters to the output of the delay circuit **40**.

More specifically, transistors **42**, **52** and **50** combine with resistor **44** to form a constant current source when the input to the delay circuit is at a high voltage. In this state, transistor **50** draws current through resistor **44** which turns on the current mirror formed by transistors **42** and **52**. In the preferred embodiment, Vdd is about 5 volts and R44 is approximately 84 Kohms which defines the current through transistor **42** at about 40 microamps. Transistor **42** has an w/l (area) of 180/9 and transistor **52** has an w/l (area) of 9/9. Thus, the current through transistor **42** is approximately 20 times the current through transistor **52**. Thus the current in transistor **52** is approximately 2 microamps. This constant current charges capacitor **56** when the input voltage is high. In general, the time delay can be approximately described as

$$\text{time delay} = (\text{switch voltage}/V_{r44})\,(C56)\,(R44)\,(\text{current ratio})$$

where:

switch voltage=the switch voltage for the inverter

V_{r44}=the voltage drop across R44

C56=the capacitance of capacitor **56**

R44=the resistance of resistor **44**

current ratio=the current ratio of the applicable current mirror.

In an embodiment, a 10 picofarad capacitor, 84 kilo-ohm resistor, and current ratio of 20 are used which yields a delay of approximately (2.5 v/4 v) (10 pF) (84 k) (20)=10.5 microseconds. (Note that the voltage drop across resistor **44** is reduced from Vdd by the voltage drop across the transistors in the current path, which in this case totals to around 1 volts.)

Conversely, transistors **48**, **46**, and **54** combine with resistor **44** to form a constant current drain for discharging capacitor **56**. When the input of delay circuit **40** is at a low voltage, transistor **50** is off and transistor **48** is on. This allows current to flow through transistor **48** and resistor **44**, thus, turning on transistors **46** and **54**. With an 84 kohm resistor and 5 volt Vdd, the current through transistor **46** is approximately equal to 40 microamps. Transistor 46 has 20 times the area as transistor **54** so that the current through transistor **54** is about 2 microamps. Therefore, capacitor **56** is discharged at the rate of 2 microamps which creates a delay of about 10.5 microseconds when the input of delay circuit is low.

Transistors **58** and **60** are configured to invert the voltage on the capacitor **56**. When the voltage on the gates of transistors **58** and **60** are low, the voltage on output is low and vice versa. Transistors **62** and **64** are also configured as an inverter with the gates configured as the input and the drain of transistor **62** connected to the drain of transistor **64** to form the output of the inverter. The first and second inverter form the output stage of the delay circuit and buffer the voltage on the capacitor to the output of the delay circuit **40**. It is understood that numerous circuits can be used for buffering voltages without departing from the spirit and scope of the invention.

The embodiment of the invention offers the advantage providing a delay which over 12 times longer than the delay created by a prior art circuit using the same resistor and capacitor value. Alternatively, this embodiment of the invention creates the equivalent delay, but uses a resistor and/or capacitor which is approximately 12 times smaller than is required by the prior art circuit to achieve the same time delay.

FIG. **4** shows the layout of the embodiment and illustrates that 75% of the area required to implement the embodiment is used by the resistor and capacitor. The layout includes resistor **70**, p-channel transistors **72**, n-channel transistors **74**, and capacitor **76**. It can be noted that the layout is for five p-channel transistors, five n-channel transistors, one 84 kilo-ohm resistor, and one 10 picofarad capacitor and yields a 10.5 microsecond delay. The prior art delay circuit in FIG. 2 requires 4 transistors instead of 6 but only provides a delay of around 823 nanoseconds or would require a capacitor or resistor which over 12 times larger to yield the same delay. The layout in FIG. **4** shows that the extra transistors needed to implement the embodiment of the invention use much less area than the area needed to increase the resistance or capacitance by 12 times. Consequently this embodiment of the invention uses much less area than the prior art even though the invention requires 10 transistors (as compared to 4 transistors) because the transistors use much less area than capacitor or resistor which would be required. Therefore, the present invention provides relatively long delays without requiring large capacitors or resistors, without requiring a large area on an integrated circuit, and, thus, at a reduced cost relative to the prior art.

FIG. **5** discloses another embodiment which adds programmability to the delay circuit. This embodiment is constructed by having the source of p-channel MOSFET transistor **42** connected to Vdd and having its drain connected to a first end of resistor **44**. The second end of resistor **44** is connected to the drain of n-channel MOSFET transistor **46**. P-channel MOSFET transistor **48** has a source connected to Vdd and a drain connected to the gate of transistor **42**. The drain of n-channel MOSFET transistor **50** is connected to the gate of transistor **46**. The sources of transistors **46** and **50** are connected to ground. The gate of transistor **48** is connected to the gate of transistor **50**, the connection of which forms the input for the circuit. The gate of transistor **42** is connected to the gates of p-channel MOSFET transistors **82, 86, 90**, and **94**. The gate of transistor **46** is connected to the gates of n-channel MOSFET transistors **84, 88, 92** and **96**. The sources of transistors **82, 86, 90**, and **94** are connected to programmable delay control circuit **80**. The drains of transistors **82, 84, 86, 88, 90, 92, 94**, and **96** are connected to each other and the first plate of capacitor **56**. The input of inverter **100** is connected to the source of transistor **82** and the output of inverter **100** is connected to the source of transistor **84**. Similarly, the inputs of inverters **102, 104**, and **106** are connected to the sources of transistors **86, 90**, and